

SCREAM SINGLE CCD READOUT MODULE

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ABSTRACT

The SCREAM project (Single CCD Readout Module) was initiated to design a compact low-cost, 2-channel single charge-coupled device (CCD) readout system. A C++ software program was written to test the function of a prototype readout circuit board system. During testing the prototype circuit board was found to have several repairable design problems. Based on these findings, a new readout circuit board will be fabricated after further testing of the prototype. Eventually, the SCREAM readout board will be used for testing CCDs in a test cube at Fermilab before they are installed in instrumentation.

INTRODUCTION

The goal of the SCREAM project (Single CCD Readout Module) is to design a compact low-cost, 2-channel single charge-coupled device (CCD) readout system.

The readout system of a charge-coupled device controls the movement, manipulation, and conversion of electrical charge to a digital format as shown in Figure 1. A CCD contains an integrated circuit on a photosensitive semiconducting silicon substrate. The

silicon substrate is composed of charge wells, which form a grid of electrically distinct light sensitive areas called pixels [1]. When a photon strikes a pixel, electrons can be ejected from the semiconducting silicon through the photoelectric effect [1]. Ejected electrons are then retained in positively charged bins below each pixel [2]. When the collected electrons are ready to be read out, the positive charge is shifted sequentially from capacitive bin to bin until the photoelectrons arrive at the serial shift register [3]. The serial shift register then dumps the charge of each pixel sequentially into an output amplifier, which converts the charge into a voltage. The voltage is then sent to an analog-to-digital converter (ADC). The data from the ADC is then sent to a computer to be compiled into an image based on the data from each pixel.

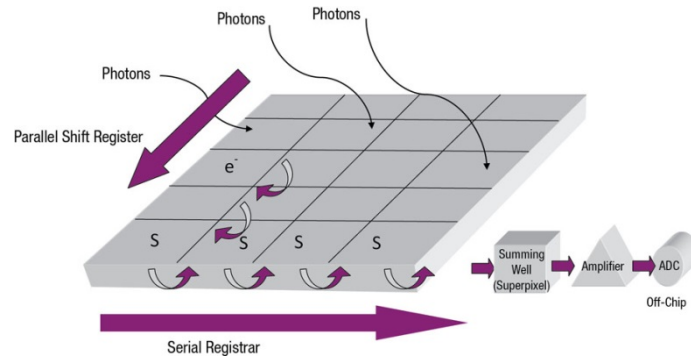


FIGURE 1: SIMPLIFIED READOUT OF A CCD

RESULTS

The Single CCD Readout Module connects to a Xilinx Virtex-6 Field Programmable Gate Array (FPGA). The FPGA is used to set clock and bias voltages and for controlling the timing of the clock voltages that are sent to the CCD for readout. The data from the CCD is temporarily stored in the FPGA memory while the CCD is being read out and is then sent to a computer connected to the FPGA.

The first part of the project involved writing a program, which allows users to send commands to the FPGA. Portions of a previously written C++ program for communicating with the Virtex-6 FPGA, written by Ryan Rivera, were used as a starting point for the current

application. The program was modified to allow the user to set and save DAC and ADC parameters in the FPGA memory and send control bits with these settings to the readout board. The DAC settings are input as voltages as shown in Appendix 1. The voltages are then converted to an 8-bit digital word that is stored in the FPGA memory until a control bit is set to send the settings to the DACs. The user interface for setting the control bits is shown in Appendix 2.

After the software was completed, it was tested to ensure that both the software and the circuit board were working properly. A multimeter and an oscilloscope were used to compare voltage outputs from the DACs with the voltage set in the software. A calibration factor was applied so that the voltage entered in the software would be the same voltage in the circuit board.

Several issues were found with the circuit board that would prevent proper operation. Two pins on the amplifiers that boost the DAC voltage for the clock voltages were swapped in the prototype board. The repair can be seen in Figure 2; 8 amplifier pin sets needed to be switched. The second major issue was that the chip, which controls the ramp up of the substrate voltage (V_{SUB}), had a different pinout than the circuit board. Most of pins had to be lifted and attached to the correct locations using wire. There were also other minor issues. DAC 2 did not have a reference voltage for its outputs. Several capacitors had to be removed because they had too long of a time constant that deformed the output wave. Several resistors had to be replaced or removed to correct DAC output voltages.

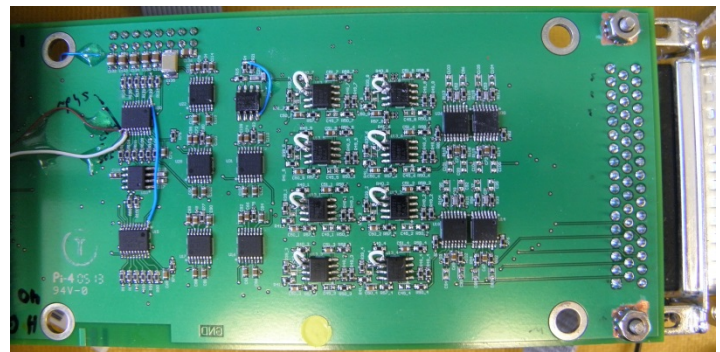


FIGURE 2: AMPLIFIER AND REFERENCE VOLTAGE FIX

The next step involved testing the sequencer. The sequencer is the part of the Xilinx FPGA that controls switching of clock voltages, which control the movement of charge through the CCD as described previously. Figure 3 shows the sequencer output for shifting the charge through the CCD. The vertical clocks being the parallel shift register and the horizontal clocks the serial shift register. The sequencer was found to operate perfectly.

FUTURE WORK

The next step in this project will be to write code to retrieve data from the ADC and compile that data into an image. Once the coding for this operation is complete, the ADC will be tested to verify that the voltage input to the readout board is converted to a digital signal that is sent to the FPGA

memory. Once that is completed, the readout board can be connected to a real CCD to see if an image is produced. When the prototype circuit board is shown to work properly, a second revised prototype readout board will be fabricated which incorporates the fixes described above. The eventual goal of the project is to have a readout module with an integrated FPGA that is user programmable and can read out many different types of CCDs.

CONCLUSION

The SCREAM Single CCD readout module will allow engineers and scientists access to a less-expensive CCD readout module. This will help reduce the cost of development and testing of CCDs used in various applications at Fermilab and at other research institutions.

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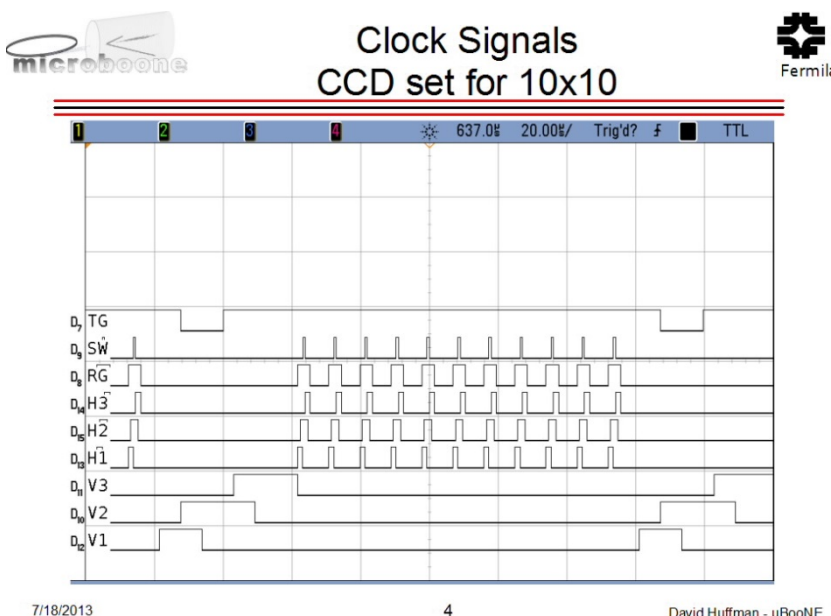
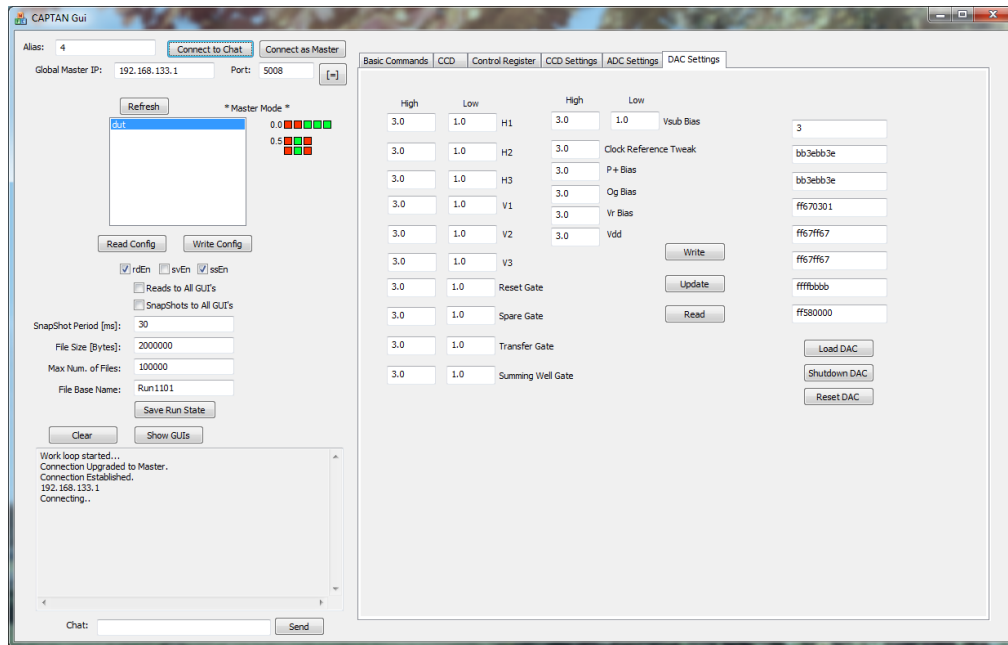
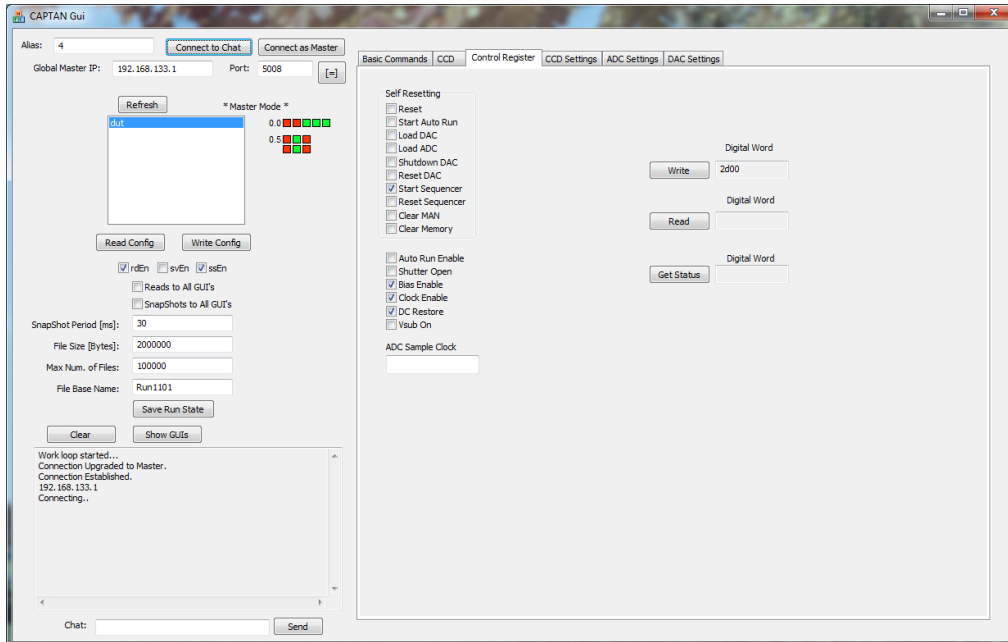


FIGURE 3: VERTICAL AND HORIZONTAL CLOCKS.

APPENDIX 1: DAC VOLTAGE TAB



APPENDIX 2: CONTROL BIT TAB



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